

TWO LEVEL CACHE MEMORY ARCHITECTURE

ABSTRACT

A memory architecture for use in a graphics processor including a main memory, a level one (L1) cache and a level two (L2) cache, coupled between the main memory and the L1 cache is disclosed. The L2 cache stores overlapping requests to the main
5 memory before the requested information is stored in the L1 cache. In this manner, overlapping requests for previously stored information is retrieved from the faster L2 cache as opposed to the relatively slower main memory.

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